



2133/J

DOCKET NO.: S01022.80854.US

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jacques PRUNIER  
Serial No: 10/083,714  
Confirmation. No.: 3976  
Filed: February 26, 2002  
For: INTEGRATED CIRCUIT TESTING METHOD AND SYSTEM

Examiner: Unassigned  
Art Unit: 2133

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 8<sup>th</sup> day of May, 2003.

William R. McClellan, Reg. No. : 29,409

Commissioner For Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

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Transmitted herewith are the following documents:

Technology Center 2100

Preliminary Amendment  
 Return Receipt Postcard

The fee has been calculated as shown below:

## CLAMS AS AMENDED

	Claims Remaining After Amendment	Highest No. Previously Paid For	Present Extra	Rate	Addl. Fee
TOTAL CLAIMS	26 -	20 =	6 X	\$ 18.00 =	\$ 108.00
INDEP. CLAIMS	3 -	3 =	0 X	\$ 84.00 =	\$ 0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					= \$ 108.00

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If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned at (617) 720-3500, Boston, Massachusetts.

A check in the amount of \$108.00 is enclosed to cover the filing fee. If the fee is insufficient, the balance may be charged to Deposit Account 23/2825. A duplicate of this sheet is enclosed.

Respectfully submitted,  
*Jacques PRUNIER, Applicant*

By: William R. McClellan  
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Telephone: (617)720-3500

Docket No. S01022.80854.US

Date: May 8, 2003

xNDDx



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William R. McClellan  
William R. McClellan, Reg. No. 29,409

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows.

In the Claims

Please amend claims 2 and 5 to read as follows. Marked-up copies of the amended claims are enclosed.

A1 2. (Amended) The integrated circuit test system of claim 1, wherein elements of a first type condition a clock signal provided to at least one flip-flop.

A2 5. (Amended) The integrated circuit test system of claim 1, wherein elements of a third type include locking elements capable of preventing the propagation of at least one signal into the logic block.

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